STABILITY AND IMPROVED CIRCUIT MODELING CONSIDERATIONS FOR HIGH POWER MMIC AMPLIFIERS

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ABSTRACT

The cluster matching approach for large periphery power FETs brings with it certain problems including more complex circuitry and new modes of possible oscillations. This paper offers some solutions to these problems including an analysis of the modes along with methods of suppression and improved circuit modeling. These solutions were implemented in the design of a two-stage, 1.6 W monolithic power amplifier which will also be discussed.

INTRODUCTION

To ensure first time success in the design of monolithic power (>1 W) amplifiers, a knowledge of certain inherent pitfalls is required. In order to achieve broadband performance from a large periphery power FET, design techniques such as cluster matching [1], [2] must be used. The cluster matching approach brings along with it certain problems including more complex circuitry and new modes of possible oscillations. This paper addresses these problems and offers some solutions. These solutions were implemented in the design of a two-stage, 1.6 W monolithic power amplifier which will also be discussed.

CLUSTER MATCHING

The cluster matching approach is routinely used in monolithic power amplifier design. In this technique, a large periphery power FET is subdivided into several identical but much smaller FETs (typically on the order of 1 mm). These smaller FETs are partially matched and eventually combined together. The combining circuitry also completes the impedance matching. One advantage of the technique is that the impedance levels of the smaller FETs are much higher than the aggregate FET and are, therefore, easier to match over a broad bandwidth. The second advantage of the technique lies in the more uniform phasing across the aggregate FET due to the identical phasing at each of the smaller FETs.

There are, however, several potential problems with the technique. Principally, the use of matching circuitry at each of the smaller FETs means that the overall matching network becomes larger and more complex. Layout constraints with the larger circuitry typically forces the smaller FETs to be widely separated. This, in turn, gives rise to the first potential problem, odd mode oscillations. Physically separated FETs, combined together at the gate and drain terminals by bondwires, transmission lines, etc., will tend to oscillate in a push-pull fashion. A second problem area, also stemming from the circuit complexity, centers around the need for improved modeling of the passive components (transmission lines, T-junctions, MIM capacitors). Any inaccuracies in passive component modeling are magnified by the numerous individual matching circuits for each of the smaller FETs.

Each of the potential problem areas cited above, along with proposed solutions, are discussed in more detail below.

ODD MODE OSCILLATIONS

The existence of odd mode oscillations in combined FET structures has been known for some time [3]. Figure 1 shows a typical spectral output of two FETs oscillating in the odd or push-pull mode. The distinguishing characteristic of the push-pull oscillation is the predominance of the even harmonics, especially the second harmonic.

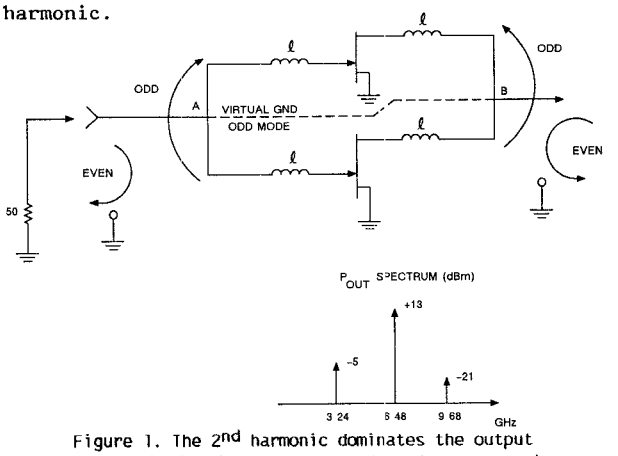

Figure 1. The 2nd harmonic dominates the output spectrum indicating odd-mode rather than even-mode oscillation. Also, a single FET alone referenced to points A and B does not oscillate.

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The FETs used to produce the spectrum in Figure 1 were combined in a FET test fixture using bondwires. The frequency of the fundamental oscillation was strongly dependent on the length of the bondwires. This fact suggests that potential oscillations could be moved away from the band of interest by judicious choice of combining points. The oscillations could then be more thoroughly suppressed by resistive loading without affecting in-band performance. A simple network for this task is shown in Figure 2(a). The series LC circuit series resonates in the band of interest thereby shorting out the loading resistor. Outside the band of interest, the loading resistor damps out any potential oscillations.

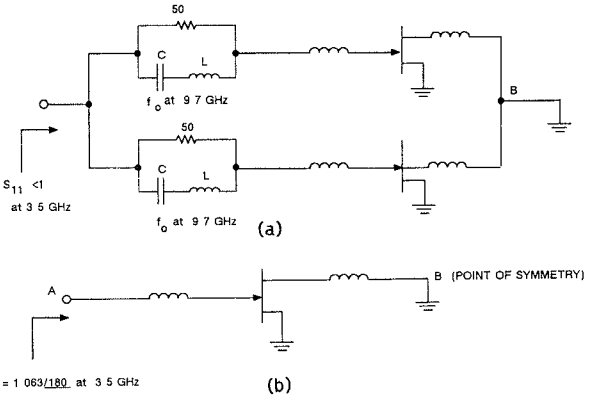

Figure 2. When the point of symmetry is shorted to ground and one half the circuit (b) analyzed, S_{11} is greater than unity; The choice of stabilizing network in (a) becomes clear and gives S_{11} less than unity.

Note, in Figure 2(b), that a method of predicting push-pull oscillations is also illustrated. Placing a short at the drain side combining point (forcing a "virtual ground"), results in an S_{11} value greater than unity with a phase angle of 180^{o} (pure resistance) at the gate side combining point at 3.5 GHz. Push-pull oscillations could, therefore, be supported at that frequency.

In-band defense against push-pull oscillations is usually needed, however. The typical approach here is to place resistors between the drains of the FETs (Figure 3). Since a push-pull oscillation creates a virtual (RF) ground at the center of the resistor, the oscillation "sees" half of the resistor value to ground. Proper choice of the resistor will therefore terminate and damp out the oscillation. Note that normal operation is not affected since equal voltages are developed across the drains resulting in zero current through the resistors.

CIRCUIT ELEMENT MODELING

Improved circuit element modeling of monolithic components is a welcome addition to any design. However, it is essential in the design of interstage circuits for multi-stage FET power amplifiers. The interstage circuit must transform the low input impedance of a FET up to the optimum large signal impedance of the preceding FET. Small errors in interstage design can cause significant loss of power output and efficiency and cause early gain compression.

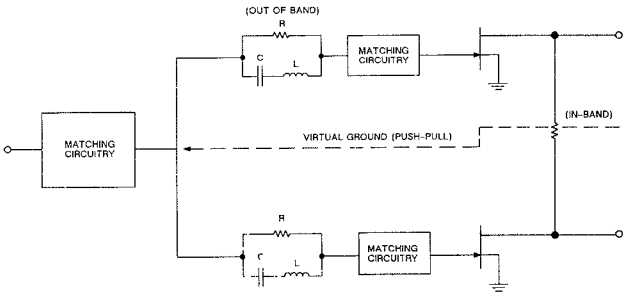

Figure 3. Push-pull oscillation suppression circuits.

Models, developed in-house, for an MIM capacitor and a microstrip T-junction are shown in Figure 4. The MIM capacitor model was motivated by considering the top and bottom plates of the capacitor as a pair of tightly coupled transmission lines over a grounded GaAs substrate [4]. Quasi- static field techniques were used to solve for the plate inductances and capacitances as a function of plate dimensions. Pi equivalent circuits of the transmission lines were then used to develop the lumped model.

The T-junction model was developed from Grover's inductance formulas for finite length lines [5]. Pi equivalent models of the microstrip lines again were used with the line capacitance values determined by standard techniques (e.g., quasi-static field) and the inductance values determined from Grover's equations. Note that an important mutual inductance between the top two branches was also included.

Grover's inductance formulas were also used for straight microstrip sections. For short length (<5 mil) 50Ω lines on 4 mil GaAs, line inductance computed by standard techniques is over-estimated by almost 100%. The difference is due to the fact that standard techniques calculate inductance/unit length based on an infinite line whereas Grover's formulas calculate inductance based on the exact line length given.

1.6 W EFFICIENT POWER AMPLIFIER

The design considerations and guidelines discussed above were incorporated into the design of a monolithic two-stage 1.6 W

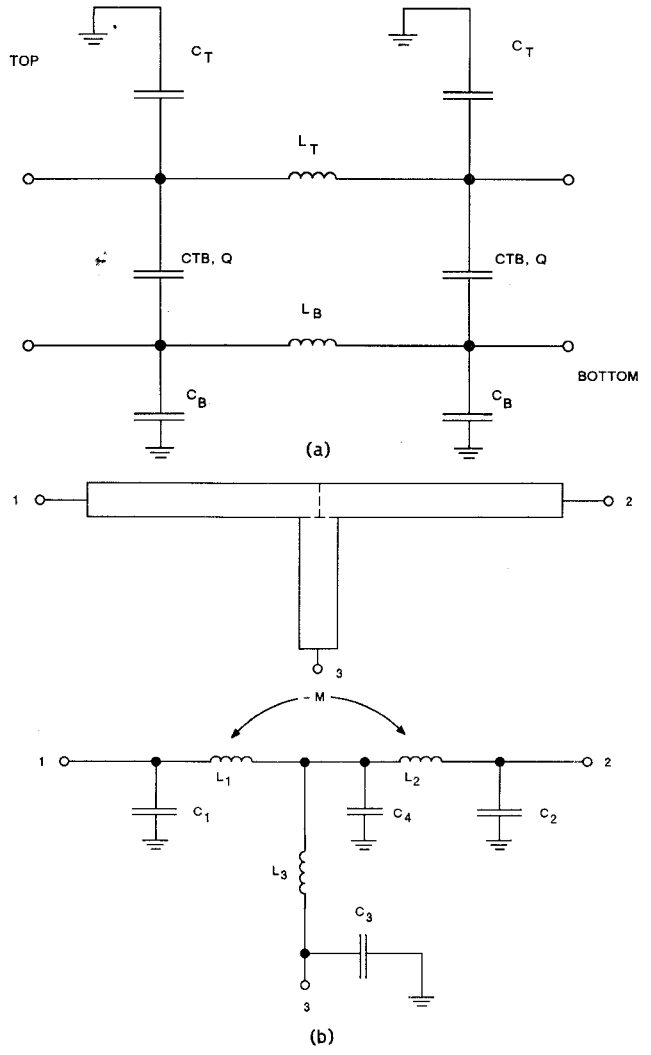

Figure 4. Improved models a) MIM capacitor and b) T-junction.

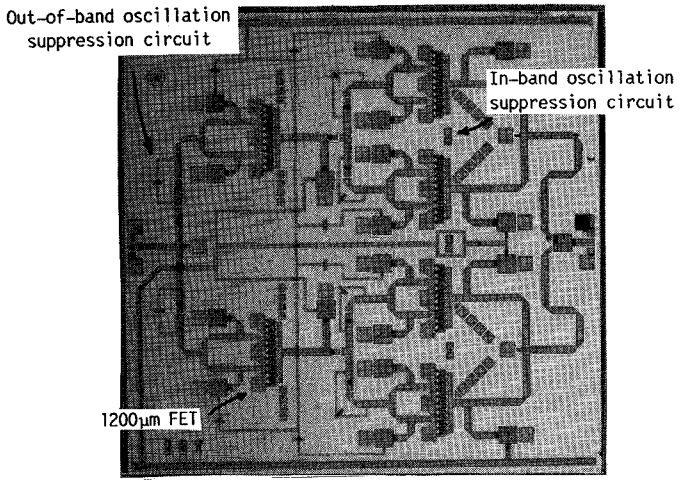

Figure 5. 1.6W MMIC power amplifier.

class AB power amplifier. A photograph of the amplifier is shown in Figure 5. The design bandwidth was 9.2 to 10.2 GHz.

Chip Device Fabrication

The LEC/PBN GaAs wafers are selectively implanted with Si ions to produce active channels for the efficient class B FETs and the damping resistors. Doping concentration of the channel is about 1.5 x $10^{17}/cm^3$. Total gate periphery of each basic FET is 1.2 mm. Each gate finger is 60μ wide and 0.9μ long. The channel is passivated with 2500A thick PECVD Si_3N_4 which also serves as the dielectric of capacitors in the circuit. The saturated drain current, I_{DSS}, is about 200 mA/mm and pinch off voltage, V_{PO}, is about 2 V. The 4μm thick plated gold serves both in transmission lines and in the airbridges. After frontside processing is completed, substrates are lapped to 4 mils thick. The sources of the FETs and shunting capacitors are grounded with chemically etched vias. For the particular circuits discussed here, the ground planes are evaporated with Cr and gold.

Circuit Design

A standard design approach, using cluster matching, was adopted for the two-stage amplifier. The output network combines the four 1200μm FETs while transforming the 50Ω load impedance to the FET optimal power impedance. The interstage network performs a similar function, transforming the input impedance of the output FET up to the optimal power impedance of the input FET. The input network was designed to match the input FET to 50Ω with a maximum 1.7:1 VSWR.

The in-band and out-of-band oscillation suppression circuits, shown in Figure 3, were included in the amplifier. Resistors were also added in the gate leads of each 1200μm FET to prevent low frequency bias line oscillations.

All of the passive element modeling (MIM capacitor, T-junction) discussed previously was used in the design process. Optimal device impedances were obtained from experimental data.

Amplifier Performance

A plot of power output and power-added efficiency versus frequency for an amplifier chip is shown in Figure 6. Between 1.6 and 1.8 W power output (9 to 9.5 dB associated gain) with >26% efficiency was obtained across the 9.2 to 10.2 GHz band. Input VSWR was better than 1.6:1 from 8.8 to 10 GHz, peaking up to 2.3:1 at 10.2 GHz.

The amplifiers, as fabricated, did not have the drain-to-drain resistors connected in so that the extra drain capacitance due to the resistor connections would be minimized. No low frequency (<7 GHz) oscillations were observed. Some chips

did exhibit push-pull oscillations at 8 GHz, however. These oscillations were damped out by connecting in the drain-to-drain resistors at the output FET and by bonding in a chip resistor between the drains of the input FET.

Measured interstage impedances (i.e., impedances presented to the first stage FET at each frequency) were very close to the design impedance, corroborating the modeling procedure.

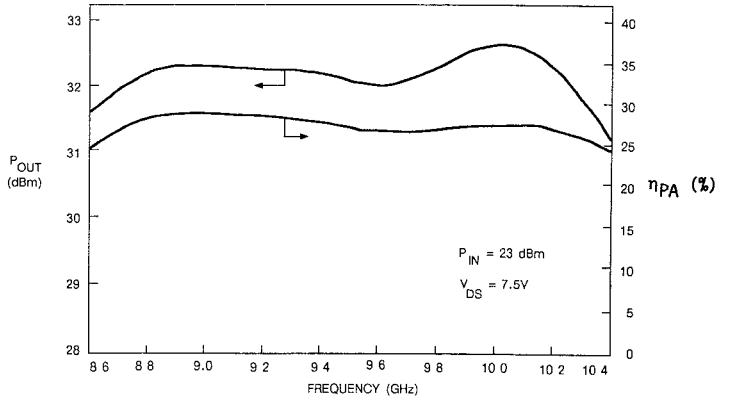

Figure 6. 1.6W MMIC performance.

CONCLUSIONS

Solutions to problems associated with cluster matching large periphery power FETs were presented. Problems included odd mode oscillations and more complex circuitry. Corresponding solutions included new oscillation suppression circuits and improved passive component modeling. Results of a two-stage, 1.6 W X-band power MMIC, using these solutions, were presented.

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